

Michael Andrew Margolese

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Interests

- Signal Integrity and Power Supply Design for High-Speed PCBs
- Radio Design (RF Front End, IF Circuits, Baseband Processing)
- Digital Signal Processing & Wireless Communications
- Automated High-Speed Digital Testing for Digital Communications
- Embedded Programming
- Embedded Systems Engineering
- Algorithm Development for Financial Market Modeling and Prediction
- Financial Time-Series Analysis
- Custom Trading Software (Automated and User Driven)

Technical Skills

- **Wireless Experience:** AMPS, CDMA(IS-95), TDMA(IS-136) protocols, QAM & QPSK Mod/Demod., FM/AM, RF Test & Measurement, Analog & Digital Circuit Design for IF & Baseband processing, Radio Systems Design & Specification for RF Cellular Responder
- **Hardware:** Xilinx Series FPGAs (All Virtex Families), Silicon Laboratories C8051F320, Motorola MC68HC11, TMS320C3X DSP, RF Test and Measurement Equipment, USB 2.0, Analog Devices AD/DACs, GPIB, Circuitry design for FPGA support (DC power, decoupling, memory interfaces, gigabit serial IO, clocking)
- **Software:** Cadence ORCAD CIS, Agilent ADS, Matlab, Simulink, Xilinx System Generator, Mathematica, UNIX OSes, Windows, HSPICE, Hyperlynx, LabWindows CVI, MathCAD, Xilinx ISE tools, some Speed2K and Ansoft HFSS, Microsoft Visual C++, Microsoft Visual Studio, PADS PCB & Logic, Windows Presentation Foundation (WPF), Windows Communication Foundation (WCF), .NET 3.5, .NET 4.0
- **Programming Languages:** Matlab, C/C++, C#, MQL4/5, LUA, Java, and Verilog
- **Licensing:** National Commodity Futures Examination Series 3

Work History

Principal Engineer

- **Employer:** Tenuvah Designs Contracted to FX Internals (<http://www.fxinternals.com>)
- **Responsibilities:**
 - Design and implementation of advanced FOREX trading interface Trader Helper
 - Design and implementation of custom trading indicators using a multiplicity of DSP techniques
 - Design and implementation of advanced mathematical analysis package for FOREX trading, including algorithms for Matrix Solving, Function Min/Max, Savitzky-Golay Filtering, Neural Networks, Wavlet Analysis, Genetic Programming for Optimization, and other proprietary techniques
 - Networking code for interfacing an SQL database, encryption, and security checking
 - Automated trading systems for high speed currency trading
- **Dates:** June 2009 to Present

Sr. Hardware Design Engineer

- **Employer:** Tenuvah Designs Contracted to L-3 Communications
- **Manager:** Juan Iturri
- **Responsibilities:**
 - Design of mixed signal control system for high current power ship board power switching system
 - Design and test of gigabit serial link for ship board power switching system
 - Signal Integrity simulations for digital PCBs
 - **Dates:** January 2008 to June 2009

Staff Design Engineer

- **Employer:** Escape Communications
- **Manager:** James Nadeau
- **Responsibilities:**
 - Layout of high speed digital radio PCBs for satellite broadband radio systems
 - Schematic capture of high speed digital radio PCBs for satellite broadband radio systems
 - **Dates:** December 2006 to May 2007

Xilinx - Senior IC Design Engineer

- **Employer:** Xilinx Inc. FPGA Labs
- **Manager:** Austin Lesea (Austin.Lesea @Xilinx.com)
- **Responsibilities:**
 - I/O & Package Characterization for Virtex-5
 - Designed high-speed characterization PCB for Sparse Chevron package testing
 - SSO noise analysis for SelectIO Standards
 - Signal & Power Integrity testing for Sparse-Chevron Package
 - Designed fully automated test setup for IO Characterization (GPIB & LUA)
 - Signal Integrity testing of all SelectIO standards for Virtex-5 family, including design of experiment (Lead Designer)
 - Single-Event-Upset testing for Virtex-4 family at Los Alamos National Labs, LANSE testing facility
 - I/O Characterization for Virtex-4 Family Launch
 - Design of experiments (Analog test & Verilog for FPGA IOB test circuits)
 - Automation of data collection and analysis through GPIB, LabWindows & LUA scripting
 - Pin to Pin testing over all IO standards supported by Virtex-4
 - SSO Noise analysis of Virtex-4 Sparse Chevron design, test results part of Xilinx's TechOnline with Howard Johnson
 - System Jitter Test Automation
 - LabWindows code to automate test setup and analysis
 - Interface code for Spectrum Analyer (HP8563E)
 - Interface code for Lecroy SDA6020 Real-Time Scope w/ Advanced Jitter Analysis
 - Interface code for Real Time Oscilloscope (TDK694C)
 - Enhanced FFT functionality
 - Extended interface for automated data processing
 - PC controlled digital design for system jitter digital circuitry (LUA & GPIB)
 - Jitter Characterization of tapped delay line elements in Virtex-4 IOBs (IDELAY)
 - Presented 10Gbps Serial Interconnect Talk at Programmable World 2004 (Tel-Aviv Site)
- **Dates:** June 2004 to August 2006

Xilinx - Applications/RF Engineer I

- **Employer:** Xilinx Inc. High Speed I/O Applications
- **Manager:** Sean Koontz (Sean.Koontz@Xilinx.com)
- **Responsibilities:**
 - Specification, design, and testing of the SIPI Test Platform
 - Design of PCB for testing the effectiveness of decoupling networks for high speed high current load switching I/Os
 - Characterize and model the effects of switching logic on system jitter
 - Interoperability testing of multi-gigabit serial transceivers
 - High Speed I/O Simulation in Hyperlynx & HSPICE using OPAL tool
 - Modeling of DCI circuits
 - RocketIO Multi-Gigabit Transceiver link modeling
 - Multi-Gigabit Transceiver Interoperability testing
 - IBIS Timing Closure Modeling for Source Synchronous Interfaces
 - Provided onsite technical support for Agilent, Australia, Elbit, Elop, Elisra, & TeraChip
 - Technical Presentations on High Speed Design (Signal & Power Integrity)
- **Dates:** June 2002 to June 2004

Xilinx - Applications/RF Engineer I

- **Employer:** Xilinx Inc. Wireless Applications
- **Manager:** Thane Koontz (Thane.Koontz@Xilinx.com)
- **Responsibilities:**
 - Specification, design, and testing of the Bali Software Defined Radio Platform.
 - Design of the Bali DSP board with an interchangeable analog interface with a Virtex-II 2V6000, DDR SDRAM PC2100 memories, and a USB 2.0 interface
 - Design of a wideband, low phase noise, IF(120 MHz) processing board using Analog Devices data converters for use with the Bali DSP Board
 - Design of a wideband, low phase noise, baseband (I&Q) processing board for use with the Bali DSP Board
 - Specification and design of a QPSK modem implemented entirely in FPGA fabric
 - Design timing and carrier recovery circuits
 - Design of filters and other modulation/demodulation components
 - Developed business partnerships and visited with major Xilinx wireless customers including Ericsson, Lucent, Agilent, Analog Devices, Elantec, Filtronetics, Spectrum Signal, and others
- **Dates:** April 2000 to June 2002

RF Engineer I

- **Employer:** Sage Instruments
- **Manager:** Doug Putnam-Pite
- **Supervisor:** Dr. Doug Rosener
- **Responsibilities:**
 - Design of software and hardware for automated testing of wireless responder systems (AMPS, TDMA, CDMA)
 - RF Testing (automated test of a switching fabric PCB in the cellular band)
 - Modulation Testing (EVM, Eb/No, & other measurements)
 - Voice Quality Testing
 - Engineering support for manufacturing
 - Manufacturing test and ATP of a TDMA test unit built for Sage Instruments
 - Electromechanical Issues (cables & connectors, ESD, vibration testing, EM model of a cavity resonator problem)
 - Designed a graphical RF analysis tool & configuration software for cellular responders
 - Embedded systems programming. Project included adding PSQM to the responder, DSP and Test algorithm analysis, and participation in the specification of a Cellular/PCS band RF switchboard
- **Dates:** June 1999 to April 2000

Education & Awards

- Graduate work in Electromagnetics and Signal Processing at Santa Clara University and Stanford University
- B.S. Computer Engineering from UC Santa Cruz, Honors and Comprehensive Honors
- IEEE Student Branch Center for Excellence Grant

Publications

- Margolese, Michael A. and Blanchard, Tim "IBIS Timing Closure", Xilinx Application Note
- Margolese, Michael A. and Ferguson, Joel F. "Using Temporal Constraints for Crosstalk Candidate Reduction for Design and Test", Published at VLSI Test Symposium '99.
- Chan, Pak et al. "Reducing Compilation Time of Zhong's FPGA Based SAT Solver", Poster paper at FCCM '99.

Patents

- U.S. Patent Office Number 7,088,288 – August 8, 2006 – A method and circuit for controlling an antenna system.
- U.S. Patent Office Number 7,349,488 – March 25, 2008 – Frequency shift keying signaling for integrated circuits
- U.S. Patent Office Number 7,512,188 – March 31, 2009 - Phase shift keying signaling for integrated circuits
- U.S. Patent Office Number 7,763,861 – July 27, 2010 - Determining A Characteristic Of Atomic Particles Affecting A Programmable Logic Device

References

- **Name:** Josh Davidson
- **Email:** josh@algorithmfx.com
- **Home Phone:** Available on Request
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- **Name:** Misael Villegas
- **Email:** solidsnakeocelot@yahoo.com
- **Home Phone:** Available on Request
- **Work Phone:** 714-943-1683

- **Name:** Mark Alexander
- **Email:** Mark.Alexander@xilinx.com
- **Home Phone:** Available on Request
- **Work Phone:** 408-410-0928

- **Name:** Sean Koontz
- **Email:** Sean.Koontz@xilinx.com
- **Home Phone:** Available on Request
- **Work Phone:** 408-410-0928

- **Name:** Thane Koontz
- **Email:** thanekoontz@ngc.com
- **Home Phone:** Available on Request
- **Work Phone:** 408-857-1648

- **Name:** Prof. Stephen Petersen, UC Santa Cruz, RF and Analog circuits professor
- **Email:** petersen@cse.ucsc.edu
- **Home Phone:** 831-335-3115
- **Work Phone:** 831-459-4782

- **Name:** Dr. Renshou Dai, Sage Instruments, DSP Research Scientist, CTO
- **Email:** renshou@sageinst.com
- **Home Phone:** 831-758-8962
- **Work Phone:** 831-761-1000

- **Name:** Dr. Doug Rosener
- **Email:** Available on Request
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